VLSI for a Physical Model of Musical Instrument Oscillations.

David Rivas, Steve Watkins, Paul M. Chau

Department of ECE R-007 University of California at San Diego, La Jolla, California, 92093

david@polanski.ucsd.edu watkins@cs.ucsd.edu, chau@celece.ucsd.edu

ABSTRACT

A VLSI implementation of a physical model for musical instrument oscillation based on the McIntrye, Schumacher, and Woodhouse model is presented. This implementation utilizes a generalization of Smith's wave digital filter formulations, and is suitable for a variety of musical instrument simulations, reverberation constructions, as well as traditional digital filtering. The Woodhouse et al. model is described including Smiths additions. Salient features of the model are pointed out and a simple generalization is provided. Following is a discussion of the generalized architecture required to implement the different models including bow-string and reed-bore simulations as well as traditional digital filter operations. A discussion of the device implementation is considered and a short discussion on implementation trade-offs is provided. Results of the design choices are noted including the results of using a bit-serial design.

1. The Model and Previous Work.

McIntyre, Schumacher, and Woodhouse [McShWo83] present a model for oscillations in musical instruments that corresponds to an energy source driving a network composed of a non-linear section and a linear section. The linear section is effectively a simple lumped transmission line of length related to the period of oscillation.

The McIntyre, Shumacher, and Woodhouse model generally requires solving simultaneously a pair of equations introducing the non-linearity. By modeling the linear portion of the network as a transmission line, the interconnection between the linear and non-linear portions of the network can be modeled as impedance mismatches at ends of the transmission line. Thus a single value in the form of a reflection coefficient can be used to parameterize the effect of the non-linear section of the system [RaWhVa84]. Smith and others [Smith86] [Garnet87] have produced results in software by generating the non-linearity via simple table look-up.

In a digital implementation, the lossless transmission line becomes a simple delay loop representing the negatively and positively traveling waves in the line. Since we are modeling physical systems the connection of the two lossless lines must obey conservation properties. Modeling the connection as a standard 2-port, and using traditional current and voltage variables we can obtain following relations:

$$V_1^- = V_2^+(1-\rho) + \rho V_1^+ \tag{1a}$$

$$V_2^- = V_1^+(1+\rho) - \rho V_2^+ \tag{1b}$$

where ρ is the reflection coefficient defined by the characteristic impedances of the two transmission lines:

$$\rho = \frac{Z_1 - Z_2}{Z_1 + Z_2}$$

the + - superscripts are incoming and outgoing waves and the subscripts denote the transmission lines. This defines the standard two port adapter used extensively by Fettweis in his wave digital filter theory [Fettwe86]. Smith [Smith86] derives a very similar equation for the bow-string mechanism:

$$V_l^- = V_r^+ + \rho V_\Delta^+ \tag{2a}$$

$$V_r^- = V_l^+ + \rho V_A^+ \tag{2b}$$

with the V's representing transverse velocity of the string to the left and right of the bow, and the differential velocity of bow and string

$$V_{\Delta}^{+} = V_{bow} - (V_r^{+} + V_l^{+})$$

Note that the reflection coefficients in (2) are time varying and parameterized by the differential bow velocity. Smith has also considered the reed-bore mechanism and arrived at similar equations. Garnett [Garnet87] uses a similar structure to model the effect of piano string excitation due to the hammer.

A key to this model is to lump all losses attributed to the acoustical systems involved at the ends of the transmission line. Thus losses as a result of the physics of the medium being simulated (dispersion, string stiffness) and interactions with terminations (bridge connections, bell) become filters at the ends of the transmission line.

2. The Architecture

The design objective was to implement a general VLSI structure that could be used as a simulation engine for physical models of a variety of musical instruments. It was also decided to easily provide for traditional wave digital filter designs as well. What this really means is that an architecture is desired which allow equations 1, 2, and equations similar to them to be computed easily. What we came up with is a structure that computes:

$$V_1^- = V_2^+ + \rho V_\Delta^+ \tag{3a}$$

$$V_2^- = V_1^+ + \rho V_A^+ \tag{3b}$$

$$V_{\Delta}^{+} = V_{param} \pm (V_{1}^{+} \pm V_{2}^{+})$$
 (3c)

where the reflection coefficient is obtained from off-chip and V_{Δ}^{+} is provided off-chip to allow table look-up of ρ . V_{param} is an input parameter (such as bow velocity). Clearly (3) immediately provides for (1) or (2). This structure in fact will compute all of the previously mentioned models. Making it useful for traditional digital signal processing as well as a simulator of musical oscillations.

The first chip we have designed implements the scattering junction as defined by (3). This is accomplished with 1 two input multiplier, 2 two input adders, and 1 three input adder. The three input adder also has the capability of independently complementing two of it's inputs.

For each sample period the chip takes as data inputs: V_1^+ , V_2^+ , V_{param}^- , and ρ . Each period the chip provides as data outputs: V_1^- , V_2^- , and V_{Δ} . V_{Δ} is meant to be used as an address into a ROM/RAM that provides values of ρ .

During a clock cycle the following control signals are required: Complement V_1^+ , Complement V_2^+ , round, and overflow generate. These signals control the functionality of the device.

3. The Implementation

VLSI design today is characterized by the CAD tools available to the designer. This allows number of approaches to be taken. In our case the wave filter module was designed in two ways. The first design was implemented as a logic level schematic capture and then a standard cell was generated automatically after full logic simulation was carried out. This was accomplished with the MENTOR design tools which run on Apollo work stations. These are industrial standard tools for custom and semi custom VLSI design.

In the interest of exploring alternative methods available to us for chip design, one of the authors (Rivas) undertook a complete redesign of the device using the OCTTOOLS VLSI design tools provided by UC Berkeley [NeSaSe86] [HaMoSN86]. Each module was specified in a special logic generation language, simulated and tested independently then routed to other modules for system simulation. The entire tool set is completely integrated into the Unix operating system environment. Thus all of the traditional program maintenance tools (eq. make, RCS/SCCS) are available to the designer. In fact, the module was created via a single make file. The command "make wdf" was issued and a few hours later a layout for the module was generated. Significantly, the Berkeley design tools are available for a nominal distribution charge.

Our implementation requirements were to generate 16 bit samples at 50KHz, at a minimum, and employ the MOSIS facility for chip fabrication. The limitations that the MOSIS requirement impose affect area and packaging. In particular the pin count and die size are limited.

The MOSIS technology that is employed utilizes 3μ CMOS. This, coupled with the die size constraints, prohibits the use of fully bit-parallel arithmetic. Thus the design is a bit-serial design. The input and output wave values V_1^{\pm} , V_2^{\pm} are fully bit-serial, but the inputs V_{param} and ρ and the output V_{Δ} are fully bit-parallel. The arithmetic is done bit-serially internally except in the case of the multiplier which is a bit-serial/bit-parallel hybrid.

Utilizing the bit-serial approach the interconnection problem, ever present in VLSI design, is significantly minimized. Bit-serial architectures, inherently require fewer interconnections to functional units. The traditional bit-serial penalty is bandwidth. Since audio is a low bandwidth signal, bit-serial designs naturally apply to audio signals.

4. The Future.

A second device that includes the tapped delay lines on chip is planned. This chip will take an additional parameter as input to choose the tap that outputs a sample. This would effectively allow pitch control on chip. The filters associated with a particular model should be implemented as wave digital structures allowing for the same compute kernel to be used in their implementation. Ideally, a monolithic device could be implemented that included all the necessary filtering as well as the delay lines and scattering junctions to introduce non-linear excitations.

In fact a full computer architecture to implement this type of physical model is being investigated. The architecture consists of modules such as the one just defined and an interconnection matrix to map interconnection schemes to the machine. Multiple wave guides and filters may be interconnected to provide for the simulation of more complex acoustical networks such as coupled strings, or piano oscillations.

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